PRODUCT/PROCESS CHANGE NOTIFICATION

PCN AMS-HES/14/8507
Dated 16 Jun 2014

Qualification of Crolles Fabrication plant as second source

Table 1. Change Implementation Schedule

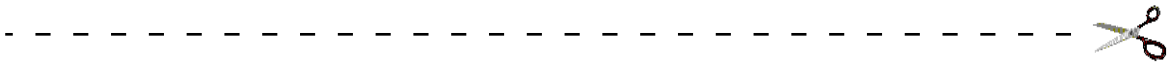
Forecasted implementation date for change	09-Jun-2014
Forecasted availability date of samples for customer	09-Jun-2014
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	09-Jun-2014
Estimated date of changed product first shipment	15-Sep-2014

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Waferfab additional location
Reason for change	To have two fabrication sites to support any upside on volume
Description of the change	Additional qualified frontend plant is activated to support demand upside
Change Product Identification	See FG's
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN AMS-HES/14/8507**
Please sign and return to STMicroelectronics Sales Office	**Dated 16 Jun 2014**
☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Lee, Wing-Sze	Marketing Manager
Italia, Francesco	Product Manager
Lisi, Giuseppe	Q.A. Manager

PRODUCT/PROCESS
CHANGE NOTIFICATION

Analog, MEMS and Sensor Group
Additional capacity for HCMOS5 and HCMOS6 (STLED316SMTR)

UMC Taiwan

ST Crolles & UMC Taiwan

WHAT:

Progressing on the activities related to HCMOS5LA and HCMOS6 technologies manufacturing expansion, ST is glad to announce additional production site in ST Crolles (France)

Material	Current process	additional process	Comment
diffusion location	UMC Taiwan	ST Crolles	No change
Wafer dimension	8 inches	8 inches	
Metallization	AlCu	AlCu	No change
Passivation	PSG/Nitride	PSG/Nitride	No change
EWS	ST Singapore	ST Singapore	No change

For the complete list of part numbers affected by the change, please refer to the attached Product list.

Samples are available, upon request.

WHY:
To improve service to ST Customers and increase capacity for the affected technologies.

HOW:
HCMOS5LA and HCMOS6 are processes already qualified in ST Crolles for other products. Extension of the line for additional AMS products is qualified based on qualification plan here attached.
Here below you'll find the details of qualification plan.

Qualification program and results:

The qualification program consists mainly of comparative electrical characterization and reliability tests. Please refer to Reliability evaluation plan for all the details.

WHEN:
Production in ST Crolles for STLED316SMTR is forecasted in Jun' 2014.

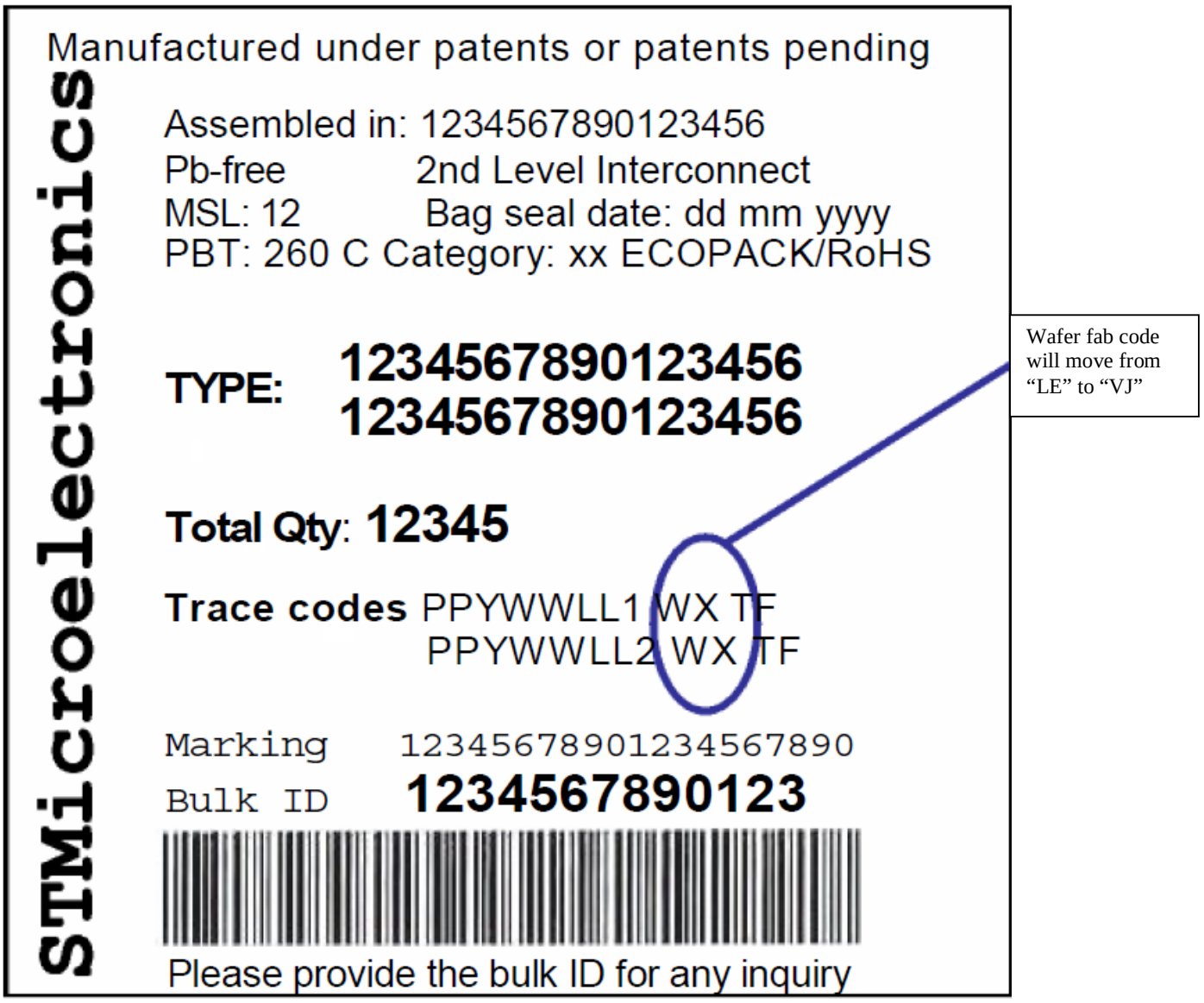
Marking and traceability:

Unless otherwise stated by customer specific requirement, the traceability of the parts assembled with the new material set will be ensured by datecode and lot number.

The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all information reported on the relevant datasheets.
There is as well no change in the packing process or in the standard delivery quantities.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).
In any case, first shipments may start earlier with customer's written agreement.

Shipments from new Wafer FAB location will be tracked on the ST Standard Label as showed below:



Generic ST Standard label

Change Qualification Plan

Double source front end plant qualification
ST Crolles HCMOS5 and HCMOS 6

Test vehicle	
Product Lines:	*V886, V632, 2012,V681*
Product Families:	• 8-bit XpanderLogic with Advanced Touch Screen Control • Micro Power rail to rail I/O Dual Op Amplifier • Stereo classD audio power amplifier • 18-bit enhanced port expander with keypad controller
P/Ns:	*STMPE811QTR,TSV632IDT,TS2012EIJT, STMPE1801*
Product Groups:	*AMS*
Product Divisions:	*HIGH-END SENSOR and ANALOG*
Packages:	*VFQFPN16 3x3x1 mm, SO8, Flip Chip*
Silicon techn.:	**Proces:** *HCMOS6, HCMOS5*

Locations	
Wafer Diffusion Plants:	*ST Crolles 200*
EWS Plants:	*ST Singapore*
Assembly Plants:	*UTAC Thai Limited, ST Bouskoura. ST Shenzhen*
T&F Plants:	*UTAC Thai Limited, ST Bouskoura, ST Shenzhen*
Reliability Lab.:	*IMS- Singapore Reliability Lab, ST Grenoble Lab*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	1-2013	15	F MURILLON	JM BUGNARD	First issue

Reference document :
RER6043-011-W-13, 14-Jan-2013, author Alfio Riciputo, Approved by Giovanni Presti
Report ID 2012-W16 H5/HF5, author X. Gagnard, approved by JM Bugnard
APM-MHD/10/5340 qualification report HCMOS5, Authors F.Murillon O. Girard, approved by F. Paccard
REL-6043-314W10 *, 16-Nov-2010, author Stefania Motta, Approved by Giovanni Presti*

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	Stress test qualification for automotive grade integrated circuits
AEC-Q101	Stress test qualification for automotive grade discrete semiconductors
AEC-Q001	Guidelines for part average testing
AEC-Q003	Guidelines for Characterizing the Electrical Performance of IC Products
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 QUALIFICATION EVALUATION OVERVIEW

3.1 Objectives

Through this qualification plan, the HCMOS5 and HCMOS6 technologies transfer is evaluated, to be diffused at Crolles.

3.2 Conclusion

Qualification Plan requirements must be fulfilled without exception. It is stressed that reliability tests must show that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests must demonstrate the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 CHANGE CHARACTERISTICS

4.1 Change description

Additional source for HCMOS5 and HCMOS6 in ST Crolles

4.2 Change details

Material	Current process	additional process	Comment
diffusion location	UMC Taiwan	ST Crolles	No change
Wafer dimension	8 inches	8 inches	
Metallization	AlCu	AlCu	No change
Passivation	PSG/Nitride	PSG/Nitride	No change
EWS	ST Singapore	ST Singapore	No change

4.3 Test vehicles description

	P/N STMPE811QTR	P/N TSV632IDT	P/N TS2012EIJT	P/N STMPE1801
Wafer/Die fab. information				
Wafer fab manufacturing location	Crolles 200	Crolles 200	Crolles 200	Crolles 200
Technology	HCMOS6LA	HCMOS5LA	HCMOS5LA	HCMOS6LA
Process family	HCMOS6	HCMOS5	HCMOS5	HCMOS6
Die finishing back side	RAW SILICON	RAW SILICON	RAW SILICON	RAW SILICON
Die size (microns)	2370x 2370 micron	1020 x 1090µm²	2150x2150µm²	203 x2030 µm²
Bond pad metallization layers	AlCu	AlCu	AlCu	AlCu
Passivation type	PSG + NITRIDE	PSG+Nitride+PIX	PSG + NITRIDE	PSG + NITRIDE
Wafer Testing (EWS) information				
Electrical testing manufacturing location	ST Singapore	ST Singapore	NA	NA
Tester	J750	ASL1000	NA	NA
Assembly information				
Assembly site	UTAC Thai	ST Bouskoura	ST Shenzhen	ST Shenzhen
Package description	VFQFPN 16 3x3x1.0	SO8	Flip Chip	Flip Chip
Molding compound	G770HCD	Sumitomo G700K	N/A	N/A
Frame material	Copper	Copper	N/A	N/A
Die attach process	Epoxy glue	Epoxy glue	N/A	N/A
Die attach material	Epoxy 8006NS	Epoxy 8601S-25	N/A	N/A
Wire bonding process	Thermosonic ball bonding	Thermosonic ball bonding	N/A	N/A
Wires bonding materials/diameters	Gold wire 1 mil	Copper wire 1 mil	N/A	N/A
Lead finishing process	Preplated frame	Preplated frame	Bump	Bump
Lead finishing/bump solder material	NiPd Pre-plated	NiPdAgAu	SnAgCu	SnAgCu
Final testing information				
Testing location	SC - UTAC Thai	ST Bouskoura	ST Shenzhen	ST Shenzhen
Tester	Credence D10	ASL1K	ASL1K	ASL3K

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Lot #	P/N	Process/ Package	Diffusion lot	Product Line	Comments
1	STMPE811QTR	HCMOS6 / QFN16 3x3	J245RTY	V886	
2	TSV632IDT	HCMOS5 / SO8	J131MAC	V632	
3	TS2012EIJT	HCMO5 / Wafer level CSP	J920FZJ	2012	
4	STMPE1801	HCMOS6 / Wafer level CSP	J013EHH	V681	

5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS				Note
						Lot 1	Lot 2	Lot 3	Lot 4	
Die Oriented Tests										
HTB High Temp. Bias	N	JESD22 A-108	Tj = 125°C, BIAS		168H 1000H	0/77 0/77	0/78 0/78	0/78 0/78	0/77 0/77	
HTSL High Temp. Storage Life	N	JESD22 A-103	Ta = 150°C		168H 1000 H	0/45 0/45	0/78 0/78		0/45 0/45	
ELFR Early Life Failure Rate	N	AEC Q100 - 008	Ta=125°C		48H		0/200			
Package oriented test										
PC Preconditioning		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Oven Reflow @ Tpeak=260°C 3 times		Final	PASS	PASS		PASS	
AC Auto Clave (Pressure Pot)	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		168 H		0/78			
TC Temperature Cycling	Y	JESD22 A-104	Ta = -65°C to 150°C		100cy 500cy		0/78 0/78	0/78 0/78	0/77 0/77	
THB Temperature Humidity Bias	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS		168H 500 H 1000 H		0/78 0/78		0/77 0/77 0/77	
Other Tests										
ESD Electro Static Discharge	-	AEC Q101-001, 002 and 005	HBM			2kV	4kV	2kV		
			MM				300V	200V		
			CDM			250V	1.5kV	750V		
LU Latch up	N	AEC Q100-004	LU			200mA	200mA			

(1) AnnexES

Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life **HTB** High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTRB High Temperature Reverse Bias **HTFB / HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
ELFR Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
THS Temperature Humidity Storage	The device is stored at controlled conditions of ambient temperature and relative humidity.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.

Test name	Description	Purpose
PTC Power & Temperature Cycling	The power and temperature cycling test is performed to determine the ability of a device to withstand alternate exposures at high and low temperature extremes with operating biases periodically applied and removed.	It is intended to simulate worst case conditions encountered in typical applications. Typical failure modes are related to parametric limits and functionality. Mechanical damage such as cracking, or breaking of the package will also be considered a failure provided such damage was not uinduced by fixturing or handling.
EV External Visual	Inspect device construction, marking and workmanship	To verify visual defects on device (form, marking,…).
LI Lead Integrity	Various tests allow determining the integrity lead/package interface and the lead itself when the lead(s) are bent due to faulty board assembly followed by rework of the part for reassembly.	This test is applicable to all throughhole devices and surface-mount devices requiring lead forming by the user.
WBP Wire Bond Pull	The wire is submitted to a pulling force (approximately normal to the surface of the die) able to achieve wire break or interface separation between ball/pad or stitch/lead.	To investigate and measure the integrity and robustness of the interface between wire and die or lead metallization
WBS Wire Bond Shear	The ball bond is submitted to a shear force (parallel to the pad area) able to cause the separation of the bonding surface between ball bond and pad area.	To investigate and measure the integrity and robustness of the bonding surface between ball bond and pad area.
DS Die Shear	This determination is based on a measure of force applied to the die, the type of failure resulting from this application of force (if failure occurs) and the visual appearance of the residual die attach media and substrate/header metallization.	The purpose of this test is to determine the integrity of materials and procedures used to attach semiconductor die or surface mounted passive elements to package headers or other substrates.
PD Physical Dimension	All physical dimension quoted in datasheet of the device are measured.	Verify physical dimensions to the applicable user device packaging specification for dimensions and tolerances.
SD Solderability	This evaluation is made on the basis of the ability of these terminations to be wetted and to produce a suitable fillet when coated by tin lead eutectic solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finishes.	The purpose of this test method is to provide a referee condition for the evaluation of the solderability of terminations (including leads up to 0.125 inch in diameter) that will be assembled using tin lead eutectic solder. These procedures will test whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly using tin lead eutectic solder.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. **CBM**: Charged Device Model **HBM**: Human Body Model **MM**: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.

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